APPLICATION		REVISION			
NEXT ASSY.	USED ON	LTR	DESCRIPTION	DATE	APPROVED
	A2200	A	PILOT PRODUCTION RELEASE	4-3-92	JEA

1.0 DESCRIPTION

Bridgette is a custom gate array IC designed for use in a wide range of Amiga computers. It implements data path routing and buffering necessary in any 68020/68030/68040 Amiga, as well as 68000 based amigas with the AA chip set. The Bridgette IC is a direct plug in replacement for the data path buffers in the A3000. Bridgette is packaged in a 100 pin plastic quad flat pack (PQFP) and provides the following functions:

- Data path (including latching) between the processor bus and chip bus
- Data path (including latching) between the processor bus and the expansion bus
- Bridging of the chip bus

Use of Bridgette in a system represents a significant cost reduction over using separate TTL parts, as well as a reduction of real estate and routing complexity.

1.1 CONFIGURATION

The device shall be configured as a standard 100 pin Plastic Quad Flat Pack (PQFP) with external dimensions as shown in Figure 1.

1.2 SOURCES

Refer to Approved Vendor List.

1.3 APPLICABLE DOCUMENTS

Commodore Engineering Policy 1.02.007 Integrated Circuit Qualification Procedure
Commodore Engineering Policy 1.02.008 Integrated Circuit Process Test Specification

COMMODORE P. N.	STATUS
391380-01	ACTIVE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
ANGLES +/- 1 DEGREE
2 PLACE DECIMALS +/- 0.02
3 PLACE DECIMALS +/- 0.010

DRAWN Mike Rivers	DATE	
SYSTEM ENG.	DATE	
TEST ENG	DATE	
COMP. ENG Drew Shannon	DATE	
CIRCUIT ENG.	DATE	

Commodore

1200 WILSON DRIVE
WEST CHESTER, PA. 19380
(215) 431-9100

TITLE: IC, SM, GATE ARRAY, BRIDGETTE

SIZE	DRAWING NUMBER
A	391380
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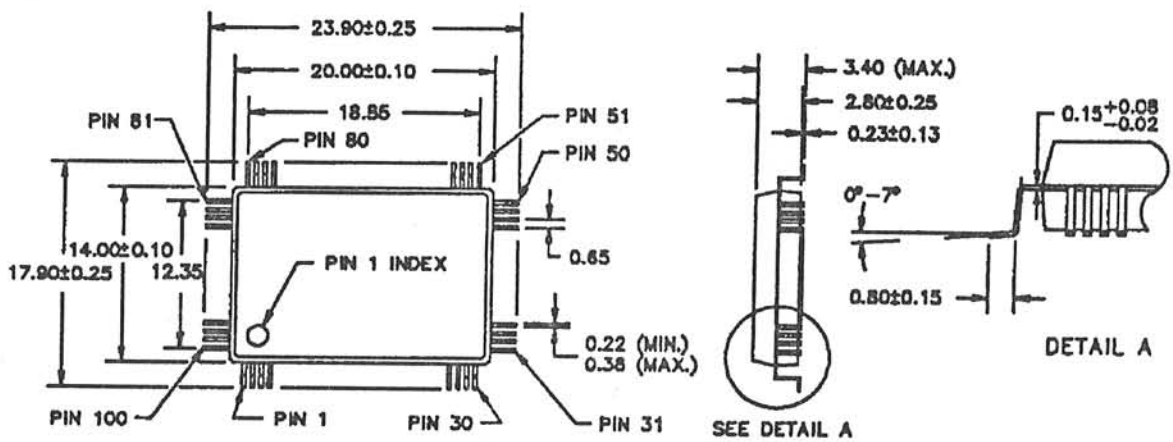
1.4 PIN DESCRIPTIONS

Group	Name	Dir	Description
Common	PD0-PD31	Bi	Processor data bus
	CD0-CD31	Bi	Custom chip data bus
	XD0-XD15	Bi	Expansion bus data bus.
Chip Bridge	CBR	Input	Signal that enables bridging of CD0-CD15 and CD16-CD31.
	CBR_DIR	Input	Determines direction that chip data bus bridge is pointing. When this signal is high data travels from CD16-CD31 to CD0-CD15, when low data travels from CD0-CD15 to CD16-CD31.
PD to XD	_XOEL	Input	Output enable the path between PD0-PD15 and XD0-XD15.
	_XOEH	Input	Output enable for the path between PD16-PD31 and XD0-XD15.
	XDIR	Input	Direction control for the data path between PD and XD. When low, data travels from XD to PD, when high data travels from PD to XD.
	XSTORED	Input	When the latch/buffer between PD16-PD31 and XD0-XD15 is set up so that data is travelling from XD to PD (XDIR low), this signal selects whether stored or real-time data is output on PD16-PD31. If XSTORED is low, real time data is output. If high, stored data is output.
	XCLK	Input	On the rising edge of XCLK, data on XD0-XD15 is clocked in, for possible later output on PD16-PD31, as described above.
CD to PD	CDIR	Input	Direction control for the buffer/latch between the chip bus and processor bus. When low, data travels from the processor bus to the chip bus, which high data travels from the chip bus to the processor bus.
	_COE	Input	Output enable for the path between the chip bus and the processor bus. If these buffers are pointing towards the CD bus, outputs are only enabled on the word of CD which the chip bridge is not pointing to, if the chip bridge buffer is enabled. If these buffers are pointing towards the PD bus, outputs are only enabled on the word of PD which a processor bridge is not pointing to, if any processor bridge buffers are enabled.
	_CLATCH	Input	This signal determines whether the data that the processor bus sees is real-time or latched chip bus data. If this signal is high, the data is real-time, if low the data is latched.



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.
2. UNLESS OTHERWISE SPECIFIED, ALL DIMENSIONS ARE NOMINAL
3. WHEN CONVERTING FROM MILLIMETERS TO INCHES, 4 SIGNIFICANT DIGITS TO THE RIGHT OF THE DECIMAL POINT ARE NECESSARY.

FIGURE 1 - PACKAGE DIMENSIONS

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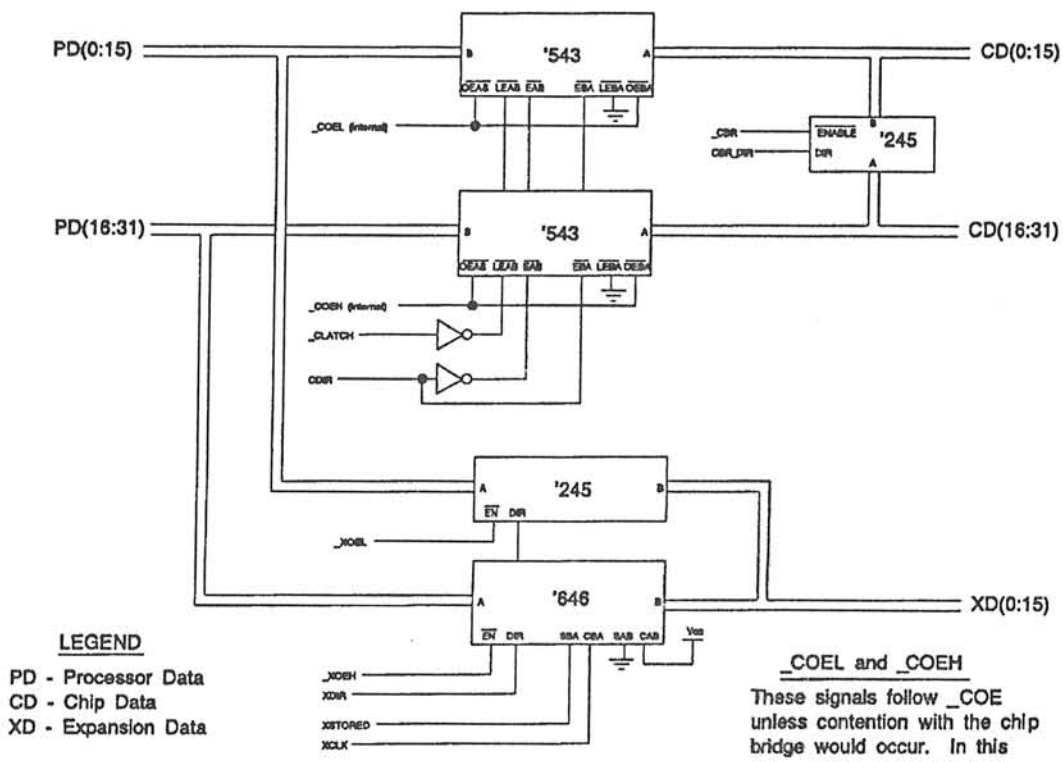
1.5 DC Characteristics

All specifications below are met over temperatures from 0 to 70C, and supply voltages of 4.5 to 5.5 volts.

PINS	PARAMETER	LIMITS MIN	LIMITS MAX	UNITS
All but _XOEH	VIH	2.0		V
All but _XOEH	VIL	0.8		V
_XOEH	VIH (VCC = 4.5V)	3.15		V
_XOEH	VIH (VCC = 5.5V)	3.85		V
_XOEH	VIL (VCC = 4.5V)		1.35	V
_XOEH	VIL (VCC = 5.5V)		1.65	V
XD0-XD15	IOL (V=0.5 max)	16		mA
XD0-XD15	IOH (V=2.5 min)	16		mA
CD0-CD31	IOL (V=0.5 max)	4		mA
CD0-CD31	IOH (V=2.5 min)	4		mA
PD0-PD31	IOL (V=0.5 max)	4		mA
PD0-PD31	IOH (V=2.5 min)	4		mA
XD0-XD15	Load capacitance	100		pF
CD0-CD31	Load capacitance	50		pF
PD0-PD31	Load capacitance	50		pF

2.0 DATA PATHS

Bridgette functionally emulates the following TTL circuit:



Commodore	TITLE: IC, SM, GATE ARRAY, BRIDGETTE			
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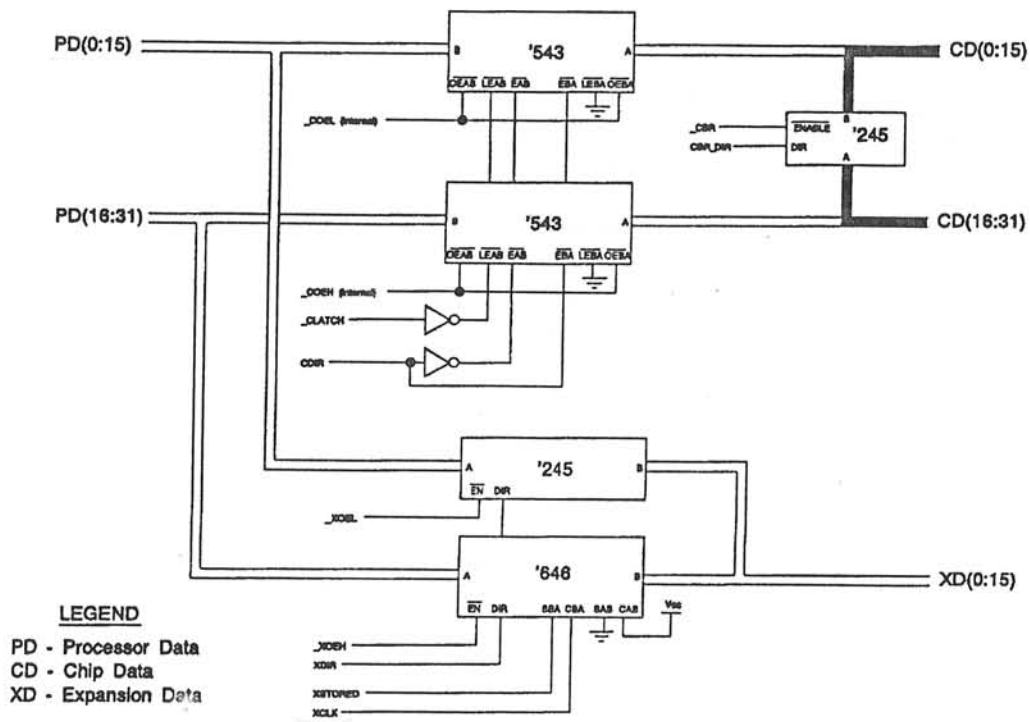
3.0 Chip Bridge Path

3.1 Data path

The data path referred to as "the chip bridge path" is shown below:



3.2 Truth table

The truth table for the chip bridge path is shown below:

Inputs		Output
_CBR	CBR_DIR	
L	L	CD(0:15) to CD(16:31)
L	H	CD(16:31) to CD(0:15)
H	X	High Z State

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3.3 Timing

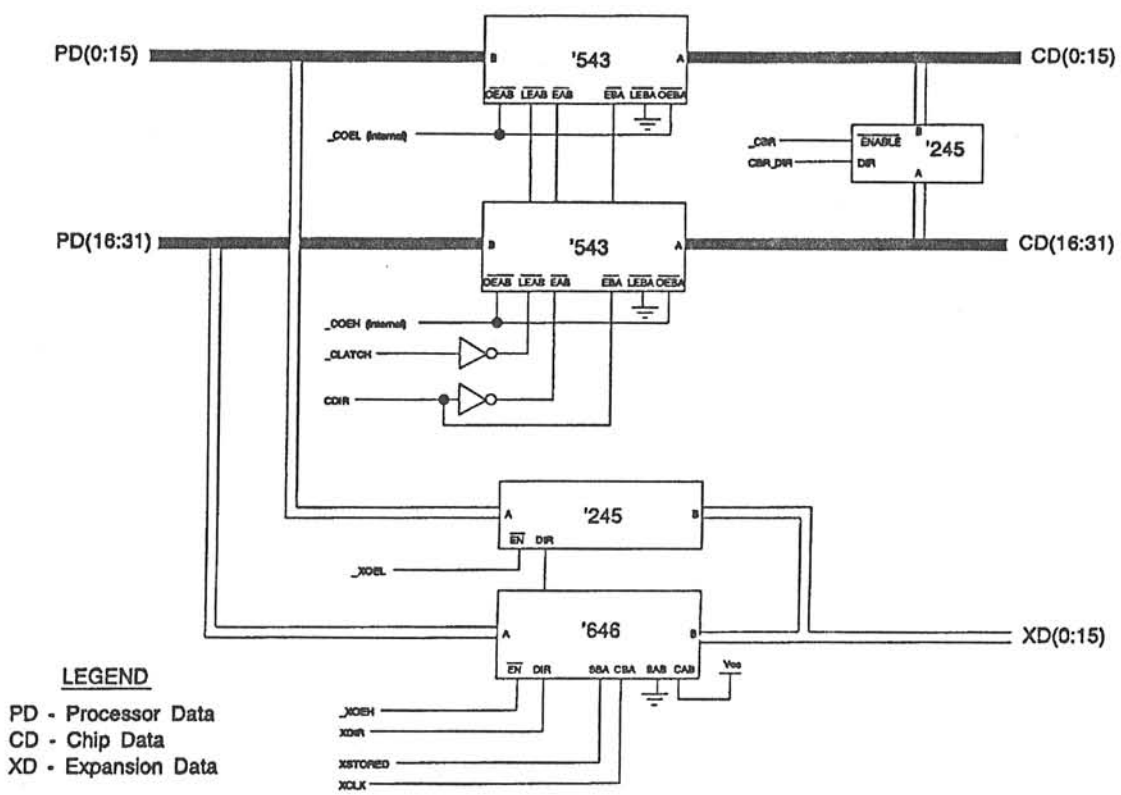
Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, CD(16:31) to CD(0:15) or CD(0:15) to CD(16:31)	13.1 ns max
Output enable time, _CBR to data valid	17.4 ns max
Output disable time, _CBR to data high Z	9.4 ns max
Direction change time, CBR_DIR to data valid	17.8 ns max

4.0 Processor to Chip Data Path

4.1 Data path

There are two paths included in this section. Most cases refer to the following path:



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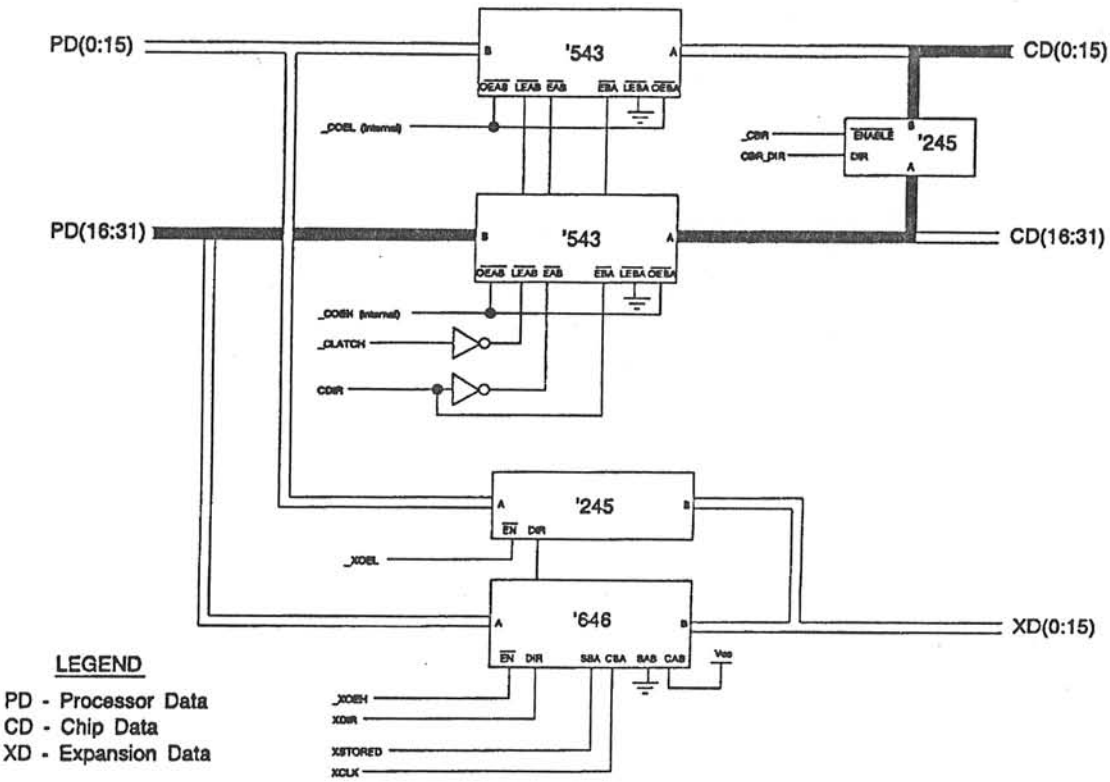
The two cases shown in the second truth table where CDIR, _COE, and _CBR are low refer to the following path:



4.2 Truth tables

The truth tables for the processor to chip data path are shown below:

Inputs			Latch Status	Output Buffers
CDIR	_CLATCH	_COE	CD to PD	PD(0:31)
L	X	X	Storing	High Z
X	L		Storing	--
X		H	--	High Z
H	H	L	Transparent	Current CD inputs
H	L	L	Storing	Previous CD inputs

Inputs				Output Buffers	
CDIR	_COE	CBR	CBR_DIR	CD(0:15)	CD(16:31)
H	X	X	X	High Z	High Z
X	H	X	X	High Z	High Z
L	L	H	X	PD(0:15)	PD(16:31)
L	L	L	H	PD(16:31)	PD(16:31)
L	L	L	L	PD(0:15)	PD(0:15)

4.3 Timing

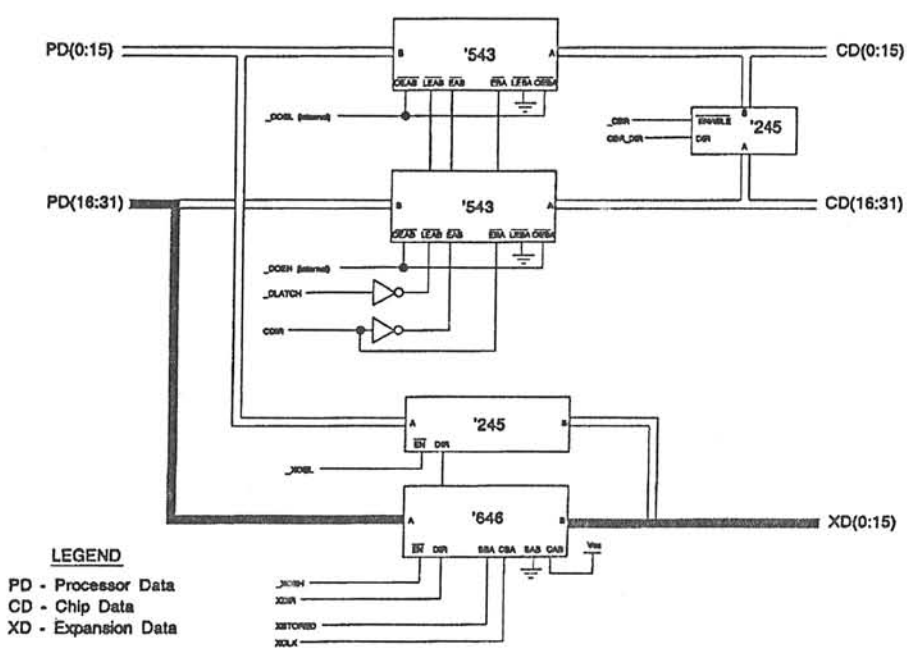
Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, transparent mode, CD0-CD31 to PD0-PD31	15.6 ns max
Propagation delay, transparent mode, PD0-PD31 to CD0-CD31	13.2 ns max
Propagation delay, CD0-CD15 to PD16-PD31	26.3 ns max
Propagation delay, PD16-PD31 to CD0-CD15	28.7 ns max
Output enable time, _COE to data valid	17.4 ns max
Output disable time, _COE to data high Z	9.4ns max
Setup time, CD to _CLATCH low	0 ns min
Hold time, _CLATCH low to data changing	3 ns min

5.0 Upper Processor Data to Expansion Data Path

5.1 Data path

The data path referred to as the "upper processor data to expansion data path" is shown below:



Commodore			TITLE: IC, SM, GATE ARRAY, BRIDGETTE	
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5.2 Truth table

The truth table for this data path is shown below:

Inputs				Data I/O		Operation or Function
_XOEH	XDIR	_XCLK	XSTORED	PD(16:31)	XD(0:15)	
H	X	H or L	X	Input	Input	Isolation
H	X	Rising	X	Input	Input	Store XD
L	L	X	L	Output	Input	Real time XD to PD
L	L	X	H	Output	Input	Stored XD to PD
L	H	X	X	Input	Output	Real time PD to XD

5.3 Timing

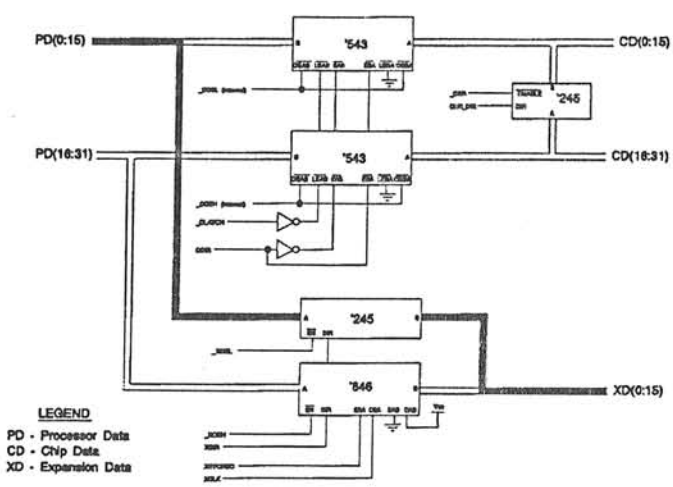
Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, PD to XD	11.4 ns max
Propagation delay, XD to PD	13.6 ns max
Output enable time, _XOEH to PD data valid	17.1 ns max
Output enable time, _XOEH to XD data valid	10.3 ns max
Output disable time, _XOEH to PD data high Z	5.8 ns max
Output disable time, _XOEH to XD data high Z	8.9 ns max
Data direction time, XDIR falling to PD data valid	19.1 ns max
Data direction time, XDIR rising to XD data valid	22.6 ns max
Setup time, XD to XCLK rising	0 ns min
Hold time, XCLK rising to data changing	2 ns min6.0

6.1 Lower Processor Data to Expansion Data Path

Data path

The data path referred to as "the lower processor data to expansion data path" is shown below:



Commodore			TITLE: IC, SM, GATE ARRAY, BRIDGETTE	
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6.2 Truth table

The truth table for the lower processor data to expansion data path is shown below:

Inputs		Output
XOEL	XDIR	
L	L	XD(0:15) to PD(0:15)
L	H	PD(0:15) to XD(0:15)
H	X	High Z State

6.3 Timing

Timing specifications for this path are shown below. In all cases, timings shown are worst case, over full rated temperature and voltage.

Propagation delay, XD(0:15) to PD(0:15)	13.4 ns max
Propagation delay, PD(0:15) to XD(0:15)	11.4 ns max
Output enable time, _XOEL to XD data valid	13.4 ns max
Output enable time, _XOEL to PD data valid	18.1 ns max
Output disable time, _XOEL to XD data high Z	9.0 ns max
Output disable time, _XOEL to PD data high Z	10.4 ns max
Direction change time, XDIR falling to PD data valid	21.8 ns max
Direction change time, XDIR rising to XD data valid	22.6 ns max

7.0 PHYSICAL REQUIREMENTS

7.1 MARKING

Parts shall be marked with Manufacturer's Part Number, Manufacturer's Identification, and EIA Date Code.

7.2 PACKAGING

The interconnected logic circuitry shall be contained in a 100-pin PQFP plastic package with exterior dimensions per Figure 1.

8.0 ENVIRONMENTAL REQUIREMENTS

Units furnished to the requirements of this specification shall meet the following environmental resistance requirements (vendors shall furnish supporting documentation upon request):

Operating Temperature	0 to 70 deg. C
Operating Humidity	5 to 95% RH non-condensing
Operating Altitude	0 to 3000 meters
Storage Temperature	- 20 to + 85 deg. C
Storage Humidity	5 to 95% RH non-condensing
Storage Altitude	0 to 15,000 meters

8.1 PROCESS QUALIFICATION TESTS

Integrated circuits supplied to the requirements of this specification shall meet the requirements of Engineering Policy No. 1.02.008. Supporting documentation shall be supplied by vendor upon request.

8.2 ENVIRONMENTAL TEST CONDITIONS

Devices shall comply with the following environmental resistance tests per Commodore Engineering Policy 1.02.007.

1. Temperature/humidity (85 deg. C and 95% RH non-condensing) for 168 hours.
2. Operating life (1000 hours at 70 deg. C ambient temperature)
3. Solderability per MIL-STD-883, Method 2003
4. Pressure cooker (15 psig, 120 deg. C, and 100% RH for 24 hours)
5. Solvent resistance per MIL-STD-883, Method 2015, using water and trichloroethane
6. Solder temperature resistance (250 deg. C for five seconds)
7. ESD requirement MIL-STD 1686 Group 3

Note: Devices shall meet this specification's operating performance requirements after the above tests are completed.

8.3 MINIMUM ACCEPTANCE LEVEL

The minimum acceptance level of any lot shall be an AQL of 0.65 as defined by MIL-STD 105 single sampling techniques.

8.4 AGE OF DEVICES

Unit shall be rejected if EIA Date Code indicates an age of three (3) or more years.

APPROVED VENDOR LIST

This sheet must be removed from this document before the document is shown or transmitted to a vendor.

Commodore Part Number	Vendor	Vendor Part Number
391380-01	NCR	BRIDGETTE

Commodore	TITLE: IC, SM, GATE ARRAY, BRIDGETTE			
SIZE	DRAWING NUMBER: 391380	REV.: A	SCALE	SHEET 1 OF 1